

Notice of References Cited	Application/Control No. 10/616,021	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner Linda Wong	Art Unit 2611	Page 1 of 1

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NON-PATENT DOCUMENTS

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*	U	Wurzer et al, A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz FT Silicon Bipolar Technology, September 1999, IEEE Journal of Solid-State Circuits, Vol. 34, No. 9, 1320-1324
*	V	Savoj et al, "A 10 Gb/s CMOS Clock and Data Recovery Circuit with Frequency Division", February 2001, 2001 IEEE International Solid-State Circuits Conference, pp 78-79, 434
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.